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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,012	04/21/2004	Yasuhiro Enomoto	0309396 H8156US	5982

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EXAMINER	
YANG, RYAN R	
ART UNIT	**PAPER NUMBER**
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,012	ENOMOTO, YASUHIRO	
	Examiner	Art Unit	
	Ryan R. Yang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Amendment, filed on 10/5/2007. This action is non-final.

2. Claims 1-11 are pending in this application. Claims 1, 9 and 11 are independent claims. In the amendment filed 10/5/2007, claims 1, 3-5 and 7-11 were amended and claim 2 was canceled.

3. This application claims foreign priority dated 4/30/2003

4. The present title of the invention is "Storage device" as filed originally.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 8, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cullen et al. (5,465,304), and further in view of Yasushi (JP 403184476).

As per claim 1, Cullen et al., hereinafter Cullen, discloses a storage device comprising:

a plurality of memory blocks each including a plurality of cells in correspondence with a data length (Figure 3);

a first register for storing a first address representing a start point for storing a specific number of first data each having the same value ("storing a first address associated with said first byte and a second address associated with said second byte in a run length record associated with said compressed scanline", column 22, line 17-

20; it is noted that Cullen does not explicitly discloses registers to store addresses, however, since a register is used to store data, it would have been obvious to one of ordinary skill in the art to consider storing address is a register for the purpose of quickly storing and retrieving data),

an adder for adding second data representing the specific number of the first data each having the same value consecutively repeated in the image data to the first address so as to produce a second address (Figure 4 illustrates a first address 403 a second address 404 and an added run length data; it is noted that Cullen does not explicitly disclose an adder to derive the second the second address, however, since the second address is derived from the first address with the run length data in between, it would have been obvious to one of ordinary skill in the art to add, using an adder, the run length data to the first address for the purpose of deriving the second address);

a second register for storing the second address ("storing a first address associated with said first byte and a second address associated with said second byte in a run length record associated with said compressed scanline", column 22, line 17-20; it is noted that Cullen does not explicitly disclose registers and adder in his teaching, however, since Cullen teaches storing a first address and a second address and added run length data, it would have been obvious to one of ordinary skill in the art to use a memory devices such as a register and an adder to perform the adding function for the purpose of storing the starting and ending of a run length data).

It is noted Cullen does not explicitly teaches "a controller for controlling the specific number of cells to be selectively and simultaneously placed in a write-enable state based on the first address and the second address", however, this is known in the art as taught by Yasushi discloses a method of processing data in which a block of same data is written simultaneously [Abstract].

Thus, it would have been obvious to incorporate the teaching of Yasushi into Cullen because Cullen discloses a method of addressing run length data and Yasushi further discloses the run length (same data) could be write-enabled for the purpose of improving the processing speed.

7. As per claim 8, Cullen and Yasushi demonstrated all the elements as disclosed in the rejected claim 1, and further discloses the first data are pixel data produced by run-length coding on serial data (since the method disclosed in Cullen is for run length data).

8. As per claim 9, Cullen discloses a method for controlling a storage device that includes a plurality of memory blocks, each including a plurality of cells in correspondence with a data length, said method comprising:

storing a first address representing a start point for storing a specific number of first data each having a same value ("storing a first address associated with said first byte and a second address associated with said second byte in a run length record associated with said compressed scanline", column 22, line 17-20);

adding run-length data representing the specific number of the first data each having the same value consecutively repeated to the first address so as to produce a

second address (Figure 4 illustrates a first address 403 a second address 404 and an added run length data);

storing the second address ("storing a first address associated with said first byte and a second address associated with said second byte in a run length record associated with said compressed scanline", column 22, line 17-20.

It is noted Cullen does not explicitly teaches "controlling a number of cells in the plurality of memory blocks to be selectively and simultaneously placed in a write-enable state based on the first address and the second address", however, this is known in the art as taught by Yasushi discloses a method of processing data in which a block of same data is written simultaneously [Abstract].

Thus, it would have been obvious to incorporate the teaching of Yasushi into Cullen because Cullen discloses a method of addressing run length data and Yasushi further discloses the run length (same data) could be write-enabled for the purpose of improving the processing speed.

9. As per claim 11, Cullen and Yasushi discloses a computer readable medium having encoded thereon instructions which when executed implement a method for controlling a storage device that includes a plurality of memory blocks each including a plurality of cells in correspondence with a data length, said method comprising the limitation similar to claim 9, therefore is similarly rejected as claim 9.

10. Claims 3-4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cullen et al. (5,465,304) in view of Yasushi (JP 403184476) as applied to claim 1 above, and further in view of Okunishi et al. (US 2002/0027676).

11. As per claim 3, Cullen and Yasushi demonstrated all the elements as disclosed in the rejected claim 1.

It is noted Cullen and Yasushi do not explicitly disclose the controller selects the number of cells based on a relationship between the first address and the second address with respect to a storage unit of a plurality of storage units, which are set across the plurality of memory blocks in correspondence with the data length, however, this is known in the art as taught by Okunishi. Okunishi discloses a method in which "from the first address, all data stored in the EEPROM 20 can be read once before the second address for data having the same contents, which is stored at a plurality of addresses, is accessed without reading the same data twice", [0102].

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Okunishi into Aoki because Aoki discloses a method of coding run length data and Okunishi discloses a method of addressing run length for the purpose of shortening processing time.

12. As per claim 4, Cullen, Yasushi and Okunishi demonstrated all the elements as disclosed in the rejected claim 2, and Okunishi further discloses the controller simultaneously selects the number of cells all belonging to a specific storage unit when both of the first address and the second address belong to the specific storage unit ("from the first address, all data stored in the EEPROM 20 can be read once before the second address for data having the same contents, which is stored at a plurality of addresses, is accessed without reading the same data twice", [0102]).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Okunishi into Aoki because Aoki discloses a method of coding run length data and Okunishi discloses a method of addressing run length in order to shorten processing time.

13. As per claim 10, Cullen and Yasushi demonstrated all the elements as disclosed in the rejected claim 9.

Cullen and Yasushi disclose a method of storing run length data. It is noted that Cullen and Yasushi do not explicitly disclose the specific number of cells are defined between the first address and the second address. However, this is known in the art as taught by Okunishi. Okunishi discloses a method of address data in which "from the first address, all data stored in the EEPROM 20 can be read once before the second address for data having the same contents, which is stored at a plurality of addresses, is accessed without reading the same data twice", [0102]).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Okunishi into Cullen and Yasushi because Cullen and Yasushi disclose a method of coding run length data and Okunishi discloses a method of addressing run length in order to shorten processing time.

14. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cullen, Yasushi and Okunishi as applied to claim 3 above, and further in view of Elrod et al. (US 5,303,200).

As per claim 5, Cullen, Yasushi and Okunishi demonstrated all the elements as disclosed in the rejected claim 3.

Cullen, Yasushi and Okunishi disclose a method of storing run length data. It is noted Cullen, Yasushi and Okunishi do not explicitly disclose wherein the controller simultaneously selects the specific number of cells, a first one of which is designated by the first address, within a specific storage unit when the first address belongs to the specific storage unit but the second address is set outside of the specific storage unit. However, this is known in the art as taught by Elrod et al, hereinafter Elrod. Elrod discloses a storage device in which the same data is written into two different memory blocks (column 10, line 14-15).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Elrod into Cullen, Yasushi and Okunishi because Cullen, Yasushi and Okunish disclose a method of coding run length data and Elrod discloses a method of addressing run length data in order to access the data through different ports.

15. As per claims 6 and 7, since Elrod discloses that same data could be written into different memory blocks, it would have been obvious to one of ordinary skill at the time the invention was made to try different combination in order to access the data through different port, therefore claims 6 and 7 are similarly rejected as claim 5.

Response to Arguments

16. Applicant's arguments, see amendment, filed 10/5/2007, with respect to the rejection(s) of claim(s) 2 under Aoki and Okunishi have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Cullen and Yasushi.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan R. Yang whose telephone number is (571) 272-7666. The examiner can normally be reached on M-F 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Yang
Primary Examiner
December 26, 2007